UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/773,583	02/05/2004	Douglas A. Larson	501296.01 (30266/US)	6732

7590 01/22/2008

Kimton N. Eng, Esq.
DORSEY & WHITNEY LLP
1420 Fifth Avenue, Suite 3400
Seattle, WA 98101

EXAMINER	
DOAN, DUC T	
ART UNIT	**PAPER NUMBER**
2188	

MAIL DATE	DELIVERY MODE
01/22/2008	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

UNITED STATES PATENT AND TRADEMARK OFFICE

Commissioner for Patents
United States Patent and Trademark Office
P.O. Box 1450
Alexandria, VA 22313-1450
www.uspto.gov

BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Application Number: 10/773,583
Filing Date: February 05, 2004
Appellant(s): LARSON ET AL.

Karen Lenaburg #58571
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed 10/29/2007 appealing from the Office action mailed 12/05/2006.

(1) Real Party in interest

A statement identifying by name the real party interest is contained in the brief.

(2) Related Appeals and Interferences

The examiner is not aware of any related appeals, interferences, or judicial proceedings which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

(3) Status of Claims

The statement of the status of claims contained in the brief is correct.

(4) Status of Amendments After Final

The statement of the status of amendments contained in the brief is correct.

(5) Summary of Claimed Subject Matter

The summary of claimed subject matter contained in the brief is correct.

(6) Grounds of Rejection to be Reviewed on Appeal

The appellant's statement of the grounds of rejection to be reviewed on appeal is correct.

(7) Claims Appendix

The copy of the appealed claims contained in the Appendix to the brief is correct.

(8) Evidence Relied Upon

US 2005/0105350	Zimmerman, David	5-2005
US 6622188	Goodwin et al	9-2003
US 6907494	Zumkehr et al	5-2005

(9) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1,4,11,14-15,21,24-25,32-43 are rejected under 35 U.S.C. 103(a) as being unpatentable over Zimmerman (US 2005/0105350), in view of Goodwin et al (US 6622188), and further in view of Zumkehr (US 6901494).

As in claim 1, Zimmerman describes a memory hub for a hub-based memory module (Zimmerman's Fig 2: MMB, paragraph 17), comprising: first and second link interfaces for coupling to respective data busses; a data path coupled to the first and second link interfaces and through which data is transferred between the first and second link interfaces (Zimmerman's Fig 2, links 112 on both sides of MMB; paragraphs 15);

Zimmerman does not disclose the claim's aspect of a bidirectional data bus operable to transfer both read and write data. However, Goodwin discloses a mechanism in which multiple memory devices are connected to a bidirectional bus as depicts in Goodwin's Fig 2: Expansion devices. It would have been obvious to one of ordinary skill in the art at the time of invention to include bi directional bus mechanism as suggested by Goodwin in Zimmerman's system thereby further allow read and write data in expansion devices such as memory devices to be transferred

effectively over the same bidirectional data bus (Goodwin's column 1 lines 10-35). Zimmerman discloses first and second link interfaces for coupling to respective portions of the bus the portion of the data bus (i.e Host side and downstream sides of the links 132, 142, each segment represent a portion of the data bus). Goodwin further discloses the expansion memory #216 having the direct data path (SCL 236 through which data is transferred between the first (i.e link to expansion memory 215) and second link (i.e link to expansion memory 218) interfaces;

Zimmerman and Goodwin do not expressly disclose the claim's detail of bypath data path. However, Zumkehr's discloses a bypath data path having a write bypass circuit coupled to the direct data path and temporarily store the write data to allow read data to be transferred through the direct data path while the write data is temporarily stored, the write bypass circuit further operable to recouple the stored write data to the direct data path after the read data is transferred through the direct data path (Zumkehr's Fig 7 #730 discloses the circuits in the translator hub providing a direct data path, in which the write data received by the translator hub (Fig 2: #220) is immediately and directly forwarding to the downstream device; Zumkehr's Fig 6 discloses a multiplexer (i.e write by pass circuit) that allowing temporary stored the write data while allowing the read data to be transferred through the direct data path, directly to the upstream device; subsequently the multiplexer recouple the stored write data and sending to the downstream device; Zumkehr's column 7 lines 17-23 discloses the write command received by the translator circuit must be delayed and allowing the read command to be transferred upstream before sending the write data downstream through the same bidirectional interface link Fig 3: #350 interface link, bi directional data signals). It would have been obvious to one of ordinary skill in the art at the time of invention to include the memory controller hub circuits and methods

as suggested by Zumkehr in Zimmerman's system to allow transferring read data while temporary storing write data, thereby resulting in more efficiently usage of the memory bus in the system (Zumkehr's column 6 lines 35-60; read and write data transferring through the same bidirectional data bus Fig 3: #350 data signals).

As in claim 4, Zimmerman's Fig 5 describes a memory device interface coupled to the data path, the memory device interface for coupling data to at least one memory device to which the memory device interface can be coupled.

Claims 11,21,32,36 rejected based on the same rationale as in the rejection of claim 1.

Claims 14,24 rejected based on the same rationale as in the rejection of claim 4.

As in claim 15, Zimmerman discloses a memory controller (Fig 2: MMB) coupled to a data path through a memory controller bus (Zimmerman's Fig 2: 112); and further coupled to at least one of the plurality of memory devices through a memory device bus (MMB couples to memory device DRAM obviously vie DRAM memory device bus), a write buffer coupled to the memory controller for storing memory requests directed to the memory device coupled to the memory controller; and a cache coupled to the memory controller for storing data provided to the memory device or retrieved from the memory device (Zimmerman's paragraph 15 discloses the buffered memory modules/controller logic to store the memory requests and to store the memory data receiving from the host).

Claim 21 rejected based on the same rationale as in the rejection of claim 1.Zimmerman's Fig 1 further discloses a processor (Zimmerman's Fig 1: #20) and processor bus connecting the processor to the system controller (Zimmerman's Fig 1: #30 MCH), which obviously having associating ports connecting to peripheral devices such as memory data storage devices

(Zimmerman's Fig 2: DRAM); a memory module (Zimmerman's Fig 3a) comprising memory hub (Fig 2: MMB). The remaining limitation of claim 21 is rejected based on the same rationale as of claim 1.

Claim 25 rejected based on the same rationale as of claim 15.

As in claim 33, Zumkehr's column 7 lines 17-23 discloses the write command received by the translator circuit must be delayed and allowing the read command to be issued earlier and, to be transferred upstream before sending the write data downstream through the same bidirectional interface link Fig 3: #350 interface link, bi directional data signals.

As in claim 34, Zumkehr describes translator circuit to translate a write command to an sdram write command for the memory device, in addition to the FIFO queue for other write commands being received (Zumkehr's column 5 lines 5-12).

As in claim 35, Zimmerman discloses wherein the memory system includes a plurality of memory modules coupled in series on the memory bus (Zimmerman's Fig 2 DRAM memory modules #120, #130 in serial on the memory bus), and writing the write data to the memory location comprises writing the write data to a memory location located in a memory module located downstream of the memory module from which the read data was accessed (Zimmrman's Fig 2 discloses writing to memory module #130 located downstream from memory module #120 in which the read data is accessed by the host #110).

Claim 37 rejected based on the same rationale of claim 33.

As in claim 38, Zumkehr's describes the write buffer to temporary store write data request (zumkerhr's Fig 3: #330).

As in claim 39, the claim recites wherein providing the write data to the memory bus comprises providing the write data through at least one memory module of the memory system before decoupling the write data from the memory bus. Zumkehr further describes the write buffer in MMB is provided to temporary store data from host and thus decoupling the host to handle another accessing data on the memory bus (Zumkehr's Fig 5)

Claim 40 rejected based on the same rationale as of claim 1. Zimmerman further discloses a memory system with multiple buffered memory modules; each memory buffer module can buffer write and read command issued from the host (Fig 2: #110). Thus the host can continue issuing commands to these buffered memory modules in concurrently manner, that is the read command can be issued to memory module Fig 2: #130 before issuing the write command to memory module Fig 2: #120.

As in claim 41, the claim rejected based on the same rationale as of claim 40. Zumkehr's column 7 lines 17-23 further discloses the write command received by the translator circuit must be delayed for a time period and allowing the read command to be transferred upstream before sending the write data downstream through the same bidirectional interface link Fig 3: #350 interface link, bi directional data signals. Therefore the collision on the bi-direction data bus can be averted.

As in claims 42-43, Zumkehr discloses the write data is stored temporary in Fig 3: #330 to avoid the collision with the read data receiving from bi-directional data signal Fig 2: 350's data signals (claim 42); wherein providing the write data to the memory bus comprises providing the write data through at least one memory module of the memory system before decoupling the write data from the memory bus (claim 43; Zumkehr discloses a FIFO to temporary store write

commands (i.e sending the write data of the first write command to at least one memory module, receiving read command, storing the data of the second write command in the FIFO before decoupling and allowing the data of a read travels through the memory bus (from Fig 3: #350 data signals to the host, Fig 3: #310 data signal).

Claims 2-3,12-13,22-23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Zimmerman (US 2005/0105350), in view of Goodwin et al (US 6622188), Zumkehr (US 6901494) as applied to claims 1,11,21 respectively, and in view of Garcia et al (US 6782435).

As in claim 2, although Zumkehr's Fig 6: #650 discloses the multiplexer providing the directly data path (read data) and the bypass data path (write data), Zumkehr does not expressly disclose the claim's detail of the multiplexer. However, Garcia's Fig 2 teaches in detail a multiplex circuit comprises a multiplexer, a bypass selection signal, and a register to temporary store write data being received. It would have been obvious to one of ordinary skill in the art at the time of invention to include the temporary storage and the multiplexer circuits as suggested by Garcia in Zimmerman's system to temporary reordering the transmitting data thereby allowing accessing memory device with minimum latency and maximizing the throughput of he overall system (Garcia's column 1, lines 48-62).

As in claims 3, the claim recite wherein the write bypass circuit further comprises an input buffer having an input coupled to the data path and an output coupled to the inputs of the multiplexer and the FIFO register. The claim rejected based on the same rationale as in the rejection of claim 2.

Claims 12, 22 rejected based on the same rationale as of claim 2.

Claims 13,23 rejected based on the same rationale as of claim 3.

(10) Response to Argument

Appellant's arguments in response to the last office action have been fully considered but they are not persuasive. Examiner respectfully traverses Appellant's arguments for the following reasons:

A) Appellant's arguments regarding the rejection of claim 40 under U.S.C 35 103(a) have been fully considered but they are not persuasive.

Appellant argues that the cited references do not teach "the data bypass capabilities when a read command is issued, and before the **read latency** is met, **issuing** a write command and corresponding write data".

Examiner contends that Appellant is arguing limitations that are not in the claims. The read latency of a memory device that Appellant referring to in his argument, is well known in the art and it means the time period of several clock cycles, from the memory device received the read command (at the first clock cycle) until it provides the beginning of read data (at the n clock cycle. Data continues to be transferred in additional clock cycles, then the execution of the read command is completed). The present invention does not claim or have any limitation regarding read latency and/or requiring "issuing of a subsequent write command and before the read latency is met". Instead the claim 40 recites "scheduling a write command after the read command completion". Scheduling a write command indicates the intention to issue a write command at any time subsequently. In other words, **the scheduling event of a write command is not the same as the issuing event of a write command**, and the issuing of the write command can be issued any time subsequently. Thus claim 40 intends to cover a much broader

period of time that allowing the write command to be issued, much longer than the "before read latency is met" period. In fact, Appellant does not have any "read latency" limitation recited in the claim, perhaps and conveniently to cover a time period larger that the "read latency" period.

As discussed above, Appellant is arguing limitations that are not in the claims, this is a frivolous argument, and therefore the argument is not persuasive.

Claim 40 at best, as a whole, describes the overlapping of a read command operation and a subsequent write command operation, wherein the write command can be issued anytime during and **before the read command operation is completed**, as discussed above.

Specifically, claim 40 describes before the read command operation is completed, then scheduling a write command to write data ("before completion of the read command, schedule a write command.."), and only requires "receiving the read data on the bidirectional memory bus from the memory system; and providing the write data to the bidirectional memory bus".

Thus at best, the recited claim is interpreted such that when a write command is issued, in a pipelining manner, at a time between a read command is issued (by the memory controller) and the time the read data completely arrived at the memory controller, this write command would met the limitations recited in the claim.

Zumkehr teaches such memory system as shown in Fig 5A. The write command is issued at T5A, in a pipelining manner, between the time a read command being issued at T1A and the time the read data complete arrived at the memory controller vie RAMBUS data bus at T6A. Thus Zumkehr teaches the claim's limitations, and therefore Appellant's arguments are not persuasive.

A1) Regarding Appellant's arguments of item D in the Appeal Brief,

First, Appellant continues to argue about the "read latency" that is not in the claim, as discussed in item A above;

Second, Examiner contents that Appellant mischaracterize Zumkehr's teaching regarding the "read latency".

Appellant argues "...In contrast, Fig 5B, which includes a write buffer in the translator hub, shows that a new write command 520B following a read command 501B can be issued before the read latency of the previously issued read command 501B is met....However, the write data 527B associated with the new write command 530B remains in the memory and cannot be issued until *after* the read latency of the previously issued read command 501B is met.." and Appellant concludes "Therefore, the Zumkehr reference does not disclose or fairly suggest data bypass capabilities when a read command is issued, and before the read latency is met, issuing a write command and corresponding write (sic).

It's not clear what" issuing a write command and corresponding write" means. Examiner assumes that Appellant intends to state" issuing a write command and corresponding write data". Thus apparently Appellant misinterprets Zumkehr's teaching of the read latency value being used for write commands, and thereby Appellant further asserting that the subsequent write command and corresponding write command must occur before the ending of the previous read command operation. Although Examiner does not agree with Appellant's assertion and the mischaracterization of Zumkehr's teaching, Examiner would like to point out that Zumkehr's teaching of the previous write command and its corresponding data occurs before the ending of the previous read command, as follows:

Zumkehr 's Fig 5B clearly discloses the concept of a pipelining mechanism of at least two write commands after the previously issued read command 501B (a previously issued read command 501B issued at T1A, see Fig 5B: rambus command going to hub; a previous write command, shown in Fig 5B as 522B, this previous write command can be issued at T1A **after** issuing the previous read command, and its corresponding data can be issued at T2A to T3A **before** the read data of the 515B on the rambus data bus (Examiner notes that the timing of the previous write command on various buses of Fig 5B can easily obtained using the timing associating with the new write command and its data).

Thus Zumkehr's previous write command and its corresponding data occurs before the read data of the previous read command (i.e before the ending of the previous red command). Therefore Appellant's argument is not persuasive.

Finally, Zumkehr "read latency" time period is used by a specific memory controller logic so that it can pace apart sending out subsequent command operations. Thus this pacing time period may be arbitrary chosen mainly to satisfy pacing requirement of a specific controller/protocol (Rambus memory controller protocol). Realizing that for an actual write operation of a memory device, for example SDRAM memory device, this "read latency" period is not necessary. Zumkehr teaches of using temporary buffering of write data and bypassing circcuitry such that read data and write data of several read and write operations can be bypassing and operate in a concurrently manner.

Zumkehr's column 2 line 61 to column 3 line 50 further teaches that this delay/defer timing **requirement ("read latency") for the write operation of a specific memory controller can be reduced and eliminated (i.e met, no longer required**) by pipelining several

read and write commands/operations, and providing buffers to temporary storing write commands and their associating data, such that these write commands and their data can be written concurrently to multiple memory devices, thereby effectively, the "read latency" of the rambus memory controller is eliminated (see Zumkehr's column 3 lines 19 to 30; It's noted that other memory devices, such as SDRAMs do not require the "read latency" delay associating with the write operation). Thus Zumkehr's clearly teaches a concept of a memory system with pipelining write and read operations, using buffers for temporary store write commands and their data, thereby met the "read latency" time period of the specific rambus memory controller, and further increase the efficiently usage of the system memory bandwidth. It's further noted that Zumkehr's teaching can be readily applied to any system memory, and any memory devices, and memory controllers, see Zumkehr's column 3 line 35 to 50).

In other words, Zumker further teaches techniques such that any timing period value including value of a "read latency" can easily met by using temporary buffers and bypass circuitry.

(11) Related Proceeding(s) Appendix

No decision rendered by a court or the Board is identified by the examiner in the Related Appeals and Interferences section of this examiner's answer.

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

/ Duc T. Doan/
Duc T. Doan
Examiner
Art Unit 2188

Conferees:

/Lynne H Browne/
Lynne H Browne
Appeal Practice Specialist, TQAS
Technology Center 2100

HYUNG S. SOUGH
SUPERVISORY PATENT EXAMINER
01/18/08